AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A Local Area Network (LAN) interfacing apparatus, comprising:

an Ethernet controller, which performs a control operation for LAN interfacing;

a codec, which is coupled to the Ethernet controller and which codes and decodes transmission/reception data;

a transceiver, which is coupled to the codec and which transmits/receives data and detects data collisions on a LAN; and

a retransmission control circuit, which is coupled between the Ethernet controller and the codec, to retransmit data after a prescribed delay period when a prescribed number of collisions occur on the LAN, wherein the retransmission control circuit comprises:

a collision control unit to detect a collision and output a collision control signal;

a first switch to switch a transmission data path output from the Ethernet controller between a first path and a second path based on the collision control signal;

a buffer on the second path to store data;

a second switch coupled to the first switch along the first path and coupled to the buffer along the second path, the second switch to pass the data to the codec.

2. (Currently Amended) The apparatus of claim 1, wherein the retransmitting control circuit retransmits an n-th data all over again when the n-th data collides on the LAN, wherein n is greater than or equal to two.

3. (Currently Amended) The apparatus of claim 1, wherein the retransmission control circuit comprises:

the collision control unit to detect an (n-1)th collision and output the collision control signal, wherein n is greater than or equal to two;

a reception control unit to logically combine the collision control signal and a reception enable signal;

the first switch to switch a transmission data outputted from the Ethernet controller to one of the first path and the second path, in accordance with the collision control signal;

a serial/parallel converter to convert the transmission data outputted from the first switch along the second path into parallel data;

the buffer to store an output of the serial/parallel converter;

a parallel/serial converter to convert the transmission data stored in the buffer into serial data;

the second switch to switch the output of the first switch or the parallel/serial converter; and

a buffer control unit to control write and output operations of the transmission data stored in the buffer, wherein the prescribed number of collisions is n.

4. (Original) The apparatus of claim 3, wherein the reception control unit prevents a transmission of a next frame by outputting a reception enable signal to the Ethernet controller when the collision control signal is activated.

5. (Original) The apparatus of claim 3, wherein the collision control unit cuts off a collision signal inputted to the Ethernet controller from the codec after a prescribed number of collisions occur.

6. (Original) The apparatus of claim 3, wherein the collision control unit comprises:

a first counter to count a number of collision signals outputted from the codec;

a first logic gate to output the collision control signal by logically combining the outputs of the first counter;

a second logic gate to prevent the transmission of the collision signal to the Ethernet controller when the collision control signal is activated;

a third logic gate to clear the first counter by logically combining the collision signal and a frame success signal outputted from the Ethernet controller; and

a second counter to reset the first counter in accordance with an empty signal outputted from the buffer.

7. (Original) The apparatus of claim 6, wherein the first counter is cleared by the third logic gate before the prescribed number of collisions occur, and is cleared by the second counter after the prescribed number of collisions occur.

8. (Original) The apparatus of claim 7, wherein the first counter is a four-bit counter, the second counter is two-bit counter, and the second counter resets the first counter when the transmission data stored in the buffer is fully transmitted.

9. (Original) The apparatus of claim 6, further comprising an inverter to stop the operation of the first counter in accordance with the output of the first logic gate when the first counter is reset by the second counter.

10. (Original) The apparatus of claim 3, wherein the first switch switches the transmission data to the serial/parallel converter when fewer than the prescribed number of LAN collisions occur, and switches the transmission data to the second switch when the prescribed number of collisions occurs.

11. (Original) The apparatus of claim 10, wherein the first switch comprises:

a logic gate to logically combine a transmission enable signal outputted from the Ethernet controller with the collision control signal outputted from the collision control unit; and

a third switch to switch the transmission data to the serial/parallel converter when the transmission enable signal and the collision control signal are high-active.

12. (Original) The apparatus of claim 3, wherein the second switch switches the output of the parallel/serial converter to the codec when data is stored in the buffer and a start signal of the buffer control unit is a high level.

13. (Original) The apparatus of claim 12, wherein the second switch comprises:

a logic gate for logically combining an empty signal outputted from the buffer and the start signal of the buffer control unit; and

a third switch to switch the output of the parallel/serial converter to the codec when the empty signal and start signal are at a high level.

14. (Original) The apparatus of claim 3, wherein the buffer control unit delays the output of the transmission data stored in the buffer for a period of an integer multiple of 52μs.

15. (Original) The apparatus of claim 3, wherein the buffer control unit comprises:

a first logic gate to logically combine the collision signal outputted from the codec with the reception enable signal;

a second logic gate to logically combine the output of the first logic gate and the collision control signal to output a retransmission signal;

a delay timer, which is reset by the retransmission signal, and outputs a start signal after a prescribed delay period;

a third logic gate to logically combine a transmission enable signal outputted from the Ethernet controller and the collision control signal, and to generate a write enable signal of the buffer; and

a fourth logic gate to logically combine an inverted start signal, the collision signal, the reception enable signal, and an inverted empty signal to generate an output enable signal.

16. (Original) The apparatus of claim 15, wherein the second logic gate outputs the retransmission signal when a prescribed transmission data collides on the LAN.

17. (Currently Amended) A retransmitting control circuit of a Local Area Network (LAN) interfacing apparatus, comprising:

a collision control unit, which detects a (n-1)th collision, outputs a collision control signal, and cuts off a collision signal inputted to an Ethernet controller from a codec when the (n-1)th collision occurs, wherein n is greater than or equal to two;

a reception control unit, which stops a transmission of a next frame by outputting a reception enable signal to the Ethernet controller in response to the collision control signal;

a first switch, which switches transmission data outputted from the Ethernet controller to a first path or a second path in response to the collision control signal;

a serial/parallel converter, which is placed on the second path to convert transmission data outputted from the first switch into parallel data;

a buffer, which stores an output of the serial/parallel converter;

a parallel/serial converter, which converts an output of the buffer into parallel data;

a second switch, which is placed on the first path to switch between an output of the first switch or the parallel/serial converter; and

a buffer control unit, which controls write and output operations of the transmission data stored in the buffer.

18. (Original) The circuit of claim 17, wherein the collision control unit comprises:

a first counter to count a number of collision signals outputted from the codec;

a first logic gate to logically combine the output of the first counter to output the collision control signal;

a second logic gate, which prevents the collision signal from being inputted to the Ethernet controller when the collision signal is activated;

a third logic gate to clear the first counter by logically combining the collision signal and a frame success signal outputted from the Ethernet controller; and

a second counter to reset the first counter in response to an empty signal outputted from the buffer.

19. (Original) The circuit of claim 18, wherein the first counter is cleared by the third logic gate before the (n-1)th collision occurs, and is cleared by the second counter after the (n-1)th collision occurs.

20. (Original) The circuit of claim 18, wherein the second counter resets the first counter when the transmission data stored in the buffer is all transmitted.

21. (Original) The circuit of claim 17, wherein the first switch switches the transmission data to the serial/parallel converter when the collision control signal and the transmission enable signal outputted from the Ethernet controller are in a high level.

22. (Original) The circuit of claim 17, wherein the second switch switches the output of the parallel/serial converter to the codec when data is stored in the buffer and the start signal of the buffer control unit is at a high level.

23. (Original) The circuit of claim 22, wherein the second switch unit comprises:

a first logic gate to logically combine the empty signal outputted from the buffer with the start signal of the buffer control unit; and

a second switch to switch the output of the parallel/serial converter to the codec when the empty signal and start signal are at a high level.

24. (Original) The circuit of claim 17, wherein the buffer control unit comprises:

a NOR gate for NORing the collision signal and the reception enable signal outputted from the codec;

an AND gate for ANDing the output of the NOR gate and the collision control signal to output the retransmission signal;

a delay timer which is reset by the retransmission signal, and outputs the start signal after a prescribed delay time;

a NAND gate for NANDing the collision control signal and the transmission enable signal to generate a write enable signal of the buffer; and

an OR gate for ORing an inverted start signal, the collision signal, the reception enable signal, and an inverted empty signal to generate an output enable signal.

25. (Original) The circuit of claim 23, wherein the AND gate outputs a retransmission signal in response to the output of the NOR gate when the LAN collision occurs on some part of the sixteenth transmission data, and wherein n=16.

26. (Currently Amended) The apparatus of claim 1, wherein the retransmission control circuit outputs an n-th data packet in accordance with a back-off algorithm after collisions of n-1 data packets of a single frame, wherein n is greater than or equal to two.

27. (Original) The apparatus of claim 3, wherein the serial/parallel converter is placed on the second path and the second switch is placed on the first path.

28. (Currently Amended) The apparatus of claim 6, wherein the first and second logic gates are AND gates ~~in~~ and the third logic gate is an OR gate.

29. (Currently Amended) The apparatus of claim 15, wherein the first logic gate is a NOR gate, the second logic gate is an AND gate, the third logic date is a NAND gate, and the fourth logic gate is an OR gate, and wherein the prescribed delay period is an integer factor of 52 microseconds.

30. (Original) The circuit of claim 17, wherein the retransmission control unit is coupled to the Ethernet controller and the codec of the local area network interfacing apparatus.

31. (Original) The circuit of claim 18, wherein the first and second logic gates are an AND gate, and the third logic gate is an OR gate.

32. (Canceled)